CLAIMS:

I claim:

1. A self-aligned trench isolation method, comprising:

forming a first gate pattern on a first region of a semiconductor substrate, the first gate pattern having a first gate insulating layer pattern, a first lower gate conductive layer pattern and a gate etching stopper layer pattern that are sequentially stacked;

forming a second gate pattern on a second region spaced apart from the first region to define a border region between the first and second regions, the second gate pattern being formed to have a second gate insulating layer pattern and a second lower gate conductive layer pattern which are sequentially stacked;

removing the gate etching stopper layer pattern to expose the first lower gate conductive layer pattern;

forming first and second trench mask patterns on predetermined regions of the first and second lower gate conductive layer patterns, respectively;

etching the first and second lower gate conductive layer patterns and the first and second gate insulating layer patterns using the first and second trench mask patterns as etching masks to form first and second lower gate electrode patterns below the first and second trench mask patterns, respectively, the semiconductor substrate in the border region being etched during the etching process of the first and second lower gate conductive layer patterns to generate a groove region having a predetermined depth in the border region; and

etching the semiconductor substrate using the first and second trench mask patterns as etching masks to form trench regions, the trench region in the border region being formed to be deeper than the trench regions in the first and second regions.

2. The method of claim 1, wherein the first and second lower gate conductive layer patterns are formed of the same material layer as the semiconductor substrate.

3. The method of claim 1, wherein the gate etching stopper layer pattern is formed of a silicon oxide layer.

4. The method of claim 1, wherein forming a second gate pattern comprises:

sequentially forming a second gate insulating layer having a different thickness from the first gate insulating layer pattern and a second lower gate conductive layer on the semiconductor substrate having the first gate pattern;

forming a photoresist pattern covering the second region spaced apart from the first region on the second lower gate conductive layer; and

etching the second lower gate conductive layer using the photoresist pattern as an etching mask.

5. The method of claim 4, further comprising:

forming a hard mask layer on the second lower gate conductive layer prior to formation of the photoresist pattern;

etching the hard mask layer using the photoresist pattern as an etching mask to form a hard mask pattern; and

removing the hard mask pattern together with the gate etching stopper layer pattern.

6. The method of claim 5, wherein forming the hard mask layer comprises forming the hard mask layer from the same material layer as the gate etching stopper layer pattern.

7. The method of claim 1, wherein forming the first and second trench mask patterns comprises:

forming a trench mask layer on the semiconductor substrate where the first lower gate conductive layer pattern is exposed; and

patterning the trench mask layer.

8. The method of claim 7, wherein the trench mask layer includes at least a polishing stopper layer.

9. The method of claim 7, wherein forming the trench mask layer comprises sequentially stacking a buffer oxide layer, a polishing stopper layer, and a hard mask layer.

10. The method of claim 1, wherein etching the semiconductor substrate to form trench regions comprises:

forming a photoresist pattern on the semiconductor substrate having the groove region, the photoresist pattern being formed to cover the second region;

etching the semiconductor substrate using the photoresist pattern and the first trench mask pattern as etching masks to form a first preliminary trench region and a preliminary border trench region that is deeper than the first preliminary trench region in the first region and the border region, respectively;

removing the photoresist pattern; and

etching the semiconductor substrate using the first and second trench mask patterns as etching masks to form a first trench region and a second trench region that is shallower than the first trench region in the first and second regions respectively and to simultaneously form a border trench region which is deeper than the first and second trench regions in the border region.

11. The method of claim 1, further comprising forming isolation layers in the trench regions.

12. A method comprising:

forming a peripheral circuit gate pattern on a predetermined region of a semiconductor substrate to define a peripheral circuit region, the peripheral circuit gate pattern being formed to have a peripheral circuit gate insulating layer pattern, a first lower gate conductive layer pattern, and a gate etching stopper layer pattern that are sequentially stacked;

forming a cell gate pattern on a region spaced apart from the peripheral circuit region to define a cell array region below the cell gate pattern and to simultaneously define a border region between the peripheral circuit region and the cell array region, the cell gate pattern being formed to have a tunnel oxide layer pattern and a second lower gate conductive layer pattern that are sequentially stacked;

removing the gate etching stopper layer pattern to expose the first lower gate conductive layer pattern;

forming first and second trench mask patterns on predetermined regions of the first and second lower gate conductive layer patterns, respectively;

etching the first and second lower gate conductive layer patterns, the tunnel oxide layer pattern, and the peripheral circuit gate insulating layer pattern using the first and second trench mask patterns as etching masks to form a lower floating gate pattern and a lower gate

electrode pattern below the first and second trench mask patterns, respectively, the semiconductor substrate in the border region being etched during the etching process of the first and second lower gate conductive layer patterns to generate a groove region having a predetermined depth; and

etching the semiconductor substrate using the first and second trench mask patterns as etching masks to form trench regions, the trench region in the border region formed to be deeper than the trench regions in the peripheral circuit region and the cell array region.

13. The method of claim 12, wherein forming the cell gate pattern comprises:

sequentially forming a tunnel oxide layer having a different thickness from the peripheral circuit gate insulating layer pattern and a second lower gate conductive layer on the semiconductor substrate having the peripheral circuit gate pattern;

forming a photoresist pattern spaced apart from the peripheral circuit region on the second lower gate conductive layer to define the cell array region; and

etching the second lower gate conductive layer using the photoresist pattern as an etching mask.

14. The method of claim 13, further comprising:

forming a hard mask layer on the second lower gate conductive layer prior to formation of the photoresist pattern;

etching the hard mask layer using the photoresist pattern as an etching mask to form a hard mask pattern; and

removing the hard mask pattern together with the gate etching stopper layer pattern.

15. The method of claim 12, wherein forming the first and second trench mask patterns comprises:

forming a trench mask layer on the semiconductor substrate where the first lower gate conductive layer pattern is exposed; and

patterning the trench mask layer.

16. The method of claim 15, wherein the trench mask layer comprises at least a polishing stopper layer.

17. The method of claim 15, wherein forming the trench mask layer comprises sequentially stacking a buffer oxide layer, a polishing stopper layer, and a hard mask layer.

18. The method of claim 12, wherein etching the semiconductor substrate to form trench regions comprises:

forming a photoresist pattern covering the cell array region on the semiconductor substrate having the groove region;

etching the semiconductor substrate using the photoresist pattern and the first trench mask pattern as etching masks to form a preliminary peripheral circuit trench region and a preliminary border trench region that is deeper than the preliminary peripheral circuit trench region in the peripheral circuit region and the border region, respectively;

removing the photoresist pattern; and

etching the semiconductor substrate using the first and second trench mask patterns as etching masks to form a peripheral circuit trench region and a cell trench region that is shallower than the peripheral circuit trench region in the peripheral circuit region and the cell array region respectively and to simultaneously form a border trench region that is deeper than the peripheral circuit trench region in the border region.

19. The method of claim 12, further comprising forming isolation layers in the trench regions.

20. A semiconductor device, comprising:

a semiconductor substrate having a first region, a second region spaced apart from the first region, and a border region between the first and second regions;

a first trench region formed in the first region to define a first active region;

a second trench region formed in the second region to define a second active region; and

a border trench region formed in the border region, the border trench region deeper than the first and second trench regions.

21. The device of claim 20, wherein the first region comprises a peripheral circuit region and the second region comprises a flash memory cell array region.

22. The device of claim 20, further comprising:

a first gate insulating layer and a first lower gate electrode pattern that are sequentially stacked on the first active region; and

a second gate insulating layer and a second lower gate electrode pattern that are sequentially stacked on the second active region, the second gate insulating layer having a different thickness from the first gate insulating layer.

23. The device of claim 20, wherein the first trench region is deeper than the second trench region.

24. The device of claim 20, further comprising isolation layers that fill the first trench region, the second trench region, and the border trench region.